Computer Architecture Midterm Exam Solution

Computer Architecture Midterm Exam Solution Computer Architecture Midterm Exam Solution A Comprehensive Guide This article provides a detailed analysis of common topics covered in a computer architecture midterm exam offering solutions and explanations to help students understand the concepts and prepare for their assessments It covers key areas such as processor design memory systems instruction sets and performance evaluation I Processor Design 1 Instruction Set Architecture ISA Explain the difference between RISC and CISC architectures RISC Reduced Instruction Set Computing Emphasizes a small simple instruction set with a fixed format This allows for faster execution and simpler pipelined designs Examples ARM MIPS CISC Complex Instruction Set Computing Offers a large complex instruction set with variablelength instructions This can lead to more efficient code for complex tasks but requires more complex decoding and execution Examples x86 Intel 8086 What are the advantages and disadvantages of each architecture RISC Advantages Faster execution simpler implementation lower power consumption RISC Disadvantages May require more instructions for complex tasks potentially larger code size CISC Advantages Can handle complex tasks with fewer instructions may offer better code density CISC Disadvantages Slower execution due to complex decoding more complex hardware implementation 2 Pipeline Design Describe the stages of a typical pipelined processor Instruction Fetch Fetches the next instruction from memory Instruction Decode Decodes the instruction and fetches operands Execute Performs the operation specified by the instruction 2 Memory Access Accesses data from memory read or write Write Back Writes the result back to the register file Explain the concept of pipeline hazards and how they are handled Data Hazards When an instruction needs the result of a previous instruction that has not yet been calculated Solved using techniques like forwarding or stalling Control Hazards When a branch instruction is encountered and the pipeline needs to decide which instruction to fetch next Solved using branch prediction techniques Structural Hazards When multiple instructions try to access the same resource simultaneously Solved by designing dedicated hardware for each stage or using techniques like interleaving access 3 Processor Performance Define the terms CPI MIPS and IPC CPI Cycles Per Instruction The average number of clock cycles required to execute one instruction MIPS Millions of Instructions Per Second The rate at which instructions are executed by a processor IPC Instructions Per Cycle The average number of instructions executed per

clock cycle Explain the relationship between these metrics CPI and MIPS Inversely proportional Lower CPI leads to higher MIPS IPC and MIPS Directly proportional Higher IPC leads to higher MIPS II Memory Systems 1 Memory Hierarchy Explain the concept of memory hierarchy and its purpose A layered system of memory with different speed and cost characteristics Faster smaller memories cache are used to store frequently accessed data while slower larger memories main memory hold less frequently used data Purpose To provide fast access to data while keeping the overall cost of the system down Describe the different levels of memory hierarchy cache main memory secondary storage Cache Small fast memory that holds frequently accessed data Typically organized in multiple levels L1 L2 L3 with L1 being the fastest and smallest Main Memory RAM Larger slower memory used to hold the currently running program and 3 its data Secondary Storage Hard Disk Slowest and largest memory used for persistent storage of data and programs 2 Cache Memory Explain the principles of cache memory locality mapping replacement Locality The tendency for programs to access data and instructions close to what they recently accessed spatial locality or that they will access again soon temporal locality Mapping Determines how memory locations are mapped to cache lines direct mapping associative mapping setassociative mapping Replacement Determines which cache line to evict when a new line needs to be loaded FIFO LRU random Explain the concept of cache miss and its impact on performance Cache Miss When the requested data is not present in the cache and needs to be fetched from main memory Impact Significantly slows down program execution because main memory access is much slower than cache access 3 Virtual Memory Explain the concept of virtual memory and its advantages A technique that allows a program to use more memory than is physically available in the system by using secondary storage as an extension of RAM Advantages Allows running programs larger than physical memory provides memory protection for different processes simplifies memory management Describe the role of the page table in virtual memory management Maps virtual addresses used by the program to physical addresses used by the memory hardware Allows for efficient switching between multiple processes in memory III Instruction Sets 1 Instruction Formats Describe the common elements of an instruction format opcode operands addressing modes 4 Opcode Specifies the operation to be performed Operands Specify the data values or memory addresses involved in the operation Addressing Modes Specify how the operands are accessed immediate register direct indirect indexed Explain the benefits of different addressing modes Immediate Efficient for constants but limited in flexibility Register Fast access suitable for frequent computations Direct Simple and effective for accessing fixed memory locations Indirect Provides flexibility for accessing data through pointers Indexed Allows for efficient access to elements in arrays 2 Instruction Types Categorize different instruction types arithmetic logical data transfer control flow Arithmetic Perform mathematical operations addition subtraction multiplication division

Logical Perform bitwise operations AND OR XOR NOT Data Transfer Move data between memory and registers Control Flow Control the order of instruction execution jumps branches calls returns Explain the purpose of each instruction type and provide examples Arithmetic ADD SUB MUL DIV Logical AND OR XOR NOT Data Transfer LOAD STORE MOVE Control Flow JMP CALL RET JZ Jump if Zero JN Jump if Negative IV Performance Evaluation 1 Performance Metrics Explain the meaning of performance metrics execution time clock rate CPI MIPS IPC throughput latency Execution Time The total time taken to complete a task Clock Rate The frequency at which the processors clock cycles CPI MIPS IPC Previously defined in the processor design section Throughput The number of tasks completed per unit time Latency The time taken for a single task to complete Discuss the relationship between different performance metrics 5 Execution Time Determined by CPI clock rate and the number of instructions executed MIPS and CPI Inversely proportional Throughput and Latency Inversely proportional 2 Performance Analysis Explain how to use performance metrics to compare different computer systems By comparing metrics like CPI MIPS throughput and latency for different systems we can assess their relative performance for specific workloads Discuss the importance of benchmark programs in performance analysis Benchmark programs are standardized tasks used to assess the performance of computer systems under specific conditions They provide a fair and consistent way to compare different hardware and software configurations Conclusion This article has provided a comprehensive review of key topics in computer architecture and offered solutions to typical midterm exam questions By understanding the concepts of processor design memory systems instruction sets and performance evaluation students can develop a solid foundation for further exploration in this critical field Remember to practice solving different problems and thoroughly analyze your results to achieve a deep understanding of the material Note This is a general guide and may not cover all topics included in your specific midterm exam Consult your syllabus lecture notes and textbook for a complete understanding of the course content

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